



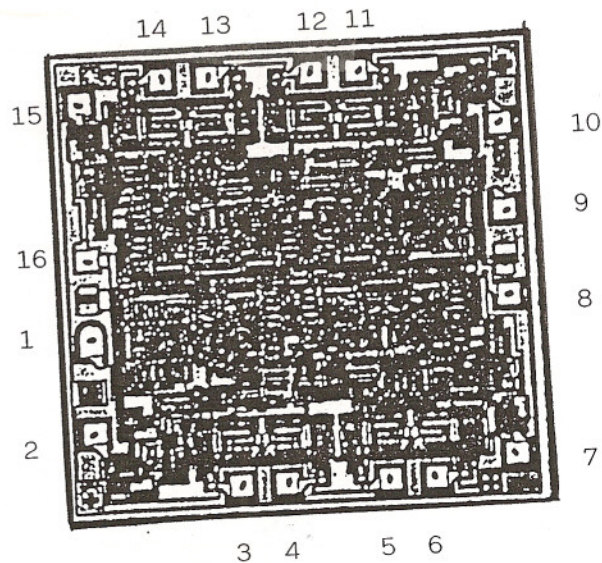
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Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

<u>PAD NO</u>	<u>FUNCTIONS</u>
1	CLOCK A
2	ENABLE A
3	Q1A
4	Q2A
5	Q3A
6	Q4A
7	RESET A
8	VSS
9	CLOCK B
10	ENABLE B
11	Q1B
12	Q2B
13	Q3B
14	Q4B
15	RESET B
16	VDD



Top Material:
Backside Material:
Bond Pad Size:
Backside Potential:
Mask Ref:

APPROVED BY:MG

DIE SIZE :86 x 86

DATE: 10/28/08

MFG:RCA

THICKNESS:

P/N:CD4518BH